IN THE SPECIFICATION

Please replace the Title of the Application with the following:

A METHOD FOR REDUCING ANTI-REFLECTIVE COATING ~~ARC~~ LAYER REMOVAL DURING REMOVAL OF PHOTORESIST

Please replace the paragraph beginning at line 13, page 1 and ending at line 1, page 2 with the following rewritten paragraph:

Figure 1 is a flow chart depicting a conventional method 10 for processing a portion of a conventional semiconductor device, such as a conventional embedded flash memory. A polysilicon layer is deposited across a semiconductor substrate, via step 12. The polysilicon layer is typically deposited on a thin insulating layer grown on the substrate. A conventional SiON anti-reflective coating ~~("ARC")~~ layer of a desired thickness is then deposited, via step 14. The conventional ~~ARC~~ anti-reflective coating layer must be deposited in a very narrow range of the desired thickness in step 14. This is because the anti-reflective properties of the conventional ~~ARC~~ anti-reflective coating layer are highly dependent upon the thickness of the conventional ~~ARC~~ anti-reflective coating layer. Typically, the desired thickness of the conventional ~~ARC~~ anti-reflective coating layer is three hundred Angstroms plus or minus ten percent (thirty Angstroms).

Please replace the paragraph beginning at line 2, page 2 with the following rewritten paragraph:

A first photoresist layer is then patterned on the conventional ~~ARC~~ anti-reflective coating layer, via step 16. The first photoresist layer pattern is typically obtained by spinning a layer of photoresist onto the ~~ARC~~ anti-reflective coating layer

and exposing portions of the photoresist layer to light through a mask layer to develop a pattern, or mask, in the photoresist layer. The first photoresist layer patterned in step 16 typically completely covers the logic region of the conventional imbedded memory. The first photoresist layer also includes a pattern over the memory region to define stacked gates in the memory region of the conventional ~~imbedded~~ embedded memory.

Please replace the paragraph beginning at line 3, page 3 with the following rewritten paragraph:

Variations in the photoresist layer thickness cause variations in the critical dimension of structures desired to be formed, otherwise known as the swing curve effect. Figure 2 is a graph 30 depicting the swing curve effect, variations in critical dimension versus photoresist thickness. The plot 31 indicates the desired size, or desired critical dimension, of a particular feature. The desired size is set by the design of the conventional embedded memory and thus is independent of resist thickness. The plot 32 depicts the variation in critical dimension versus photoresist thickness when a conventional ~~ARC~~ anti-reflective coating layer of the appropriate thickness is used. Because the conventional ~~ARC~~ anti-reflective coating layer of the appropriate thickness is used, reflections from the layer(s) underlying the photoresist layer are reduced. Thus, the structures formed using the photoresist layer have a critical dimension that is close to the desired critical dimension.

Please replace the paragraph beginning at line 14, page 3 and ending at line 1, page 4 with the following rewritten paragraph:

Curve 34 depicts the variation in the critical dimension for the structure of the desired size when no conventional ~~ARC~~ anti-reflective coating layer or a conventional ~~ARC~~ anti-reflective coating layer of an incorrect thickness is used. The anti-reflective properties of the ~~ARC~~ anti-reflective coating layer are highly

dependent on thickness of the ~~ARC~~ anti-reflective coating layer. When a resist pattern is formed without the ~~ARC~~ anti-reflective coating layer, light used in conventional photolithography may reflect off of the layer(s) and structures under the photoresist layer. The reflected light causes variations in critical dimensions of structures etched in the polysilicon layer and causes a phenomenon called reflective notching, a narrowing of the polysilicon lines as a result of reflections from the underlayer. Thus, the critical dimensions of structures fabricated with no conventional ~~ARC~~ anti-reflective coating layer or a conventional ~~ARC~~ anti-reflective coating layer without the desired thickness vary more strongly with photoresist thickness. This variation is shown in curve 34.

Please replace the paragraph beginning at line 2, page 4 with the following rewritten paragraph:

Figure 3A depicts a portion of a conventional embedded memory 40 after step 16, patterning the first resist layer, is performed. The conventional embedded memory 40 includes a logic region 44 and a memory region 42. A polysilicon layer 51 is provided on substrate 50. Note that an insulating layer (not shown) typically separates the polysilicon layer 51 from the substrate 50. In addition, underlying structures 47 and 49 are shown. Structures 47 and 49 were obtained prior to deposition of the polysilicon layer 51. A conventional ~~ARC~~ anti-reflective coating layer 52 having the desired thickness for reducing reflections is provided on the polysilicon layer 51. The thickness of the conventional ~~ARC~~ anti-reflective coating layer 52 is typically three hundred Angstroms plus or minus approximately ten percent. The first photoresist structure 53 covers the logic region 44, but defines the pattern for stacked gates in the memory region 42. Note that the first photoresist structure 53 varies in thickness.

Please replace the paragraph beginning at line 13, page 4 with the following rewritten paragraph:

Figure 3B depicts a portion of a conventional embedded memory 40 after step 18, etching gates in the memory region 42, of the method 10 shown in Figure 1 is performed. Referring to Figure 3B, stacked gates 54, 56 and 58 have been formed in the memory region 42 of the conventional embedded memory 40. The stacked gates 54, 56 and 58 are covered by remaining portions 55, 57 and 59, respectively, of the ~~ARC~~ anti-reflective coating layer 52. Portions of the first photoresist layer 53 still covers the stacked gates 54, 56 and 58 as well as the polysilicon layer 51 and the conventional ~~ARC~~ anti-reflective coating layer 52 in the logic region 44. Because the conventional ~~ARC~~ anti-reflective coating layer 52 has the desired thickness, the critical dimensions of gates 54, 56 and 58 are quite close to what is desired. In other words, variations in the critical dimension of the gates 54, 56 and 58 may follow the curve 32 depicted in Figure 2.

Please replace the paragraph beginning at line 23, page 4 and ending at line 14, page 5 with the following rewritten paragraph:

Figure 3C depicts a portion of a conventional embedded memory 40 after step 20, stripping the first photoresist structure 53, of the method 10 shown in Figure 1 is performed. Referring to Figure 3C, a portion of the conventional ~~ARC~~ anti-reflective coating layer 52 has been removed during the strip of the photoresist structure 53. Thus, the conventional ~~ARC~~ anti-reflective coating layer 52 is thinner than in Figure 3B. Typically, twenty to fifty Angstroms are removed during the wet resist strip after the etch performed in step 20. After the etch, the thickness of the conventional ~~ARC~~ anti-reflective coating layer 52 is twenty to fifty Angstroms thinner than the optimal thickness. Consequently, removal of a portion of the conventional ~~ARC~~ anti-reflective coating layer 52 during the resist strip is likely to significantly reduce the ability of the conventional ~~ARC~~ anti-reflective coating layer 52 to decrease

reflections. Thus, the gates formed in step 24 in the logic region 44 will have critical dimensions which vary greatly. In other words, the critical dimensions of structures, such as gates, in the logic region will follow the curve 44 shown in Figure 2. These large variations are undesirable. In order to reduce these variations in the logic region 44, the ~~ARC~~ anti-reflective coating layer 52 and photoresist structure 53 would be removed. The ~~ARC~~ anti-reflective coating layer 52 would then be replaced with another ~~ARC~~ anti-reflective coating layer (not shown) that is deposited at the desired thickness.

Please replace the paragraph beginning at line 15, page 5 with the following rewritten paragraph:

Accordingly, what is needed is a system and method for providing the conventional semiconductor device, such as an ~~imbedded~~ embedded memory, in which the ~~ARC~~ anti-reflective coating layer need not be removed and redeposited. The present invention addresses such a need.

Please replace the paragraph beginning at line 20, page 5 and ending at line 5, page 6 with the following rewritten paragraph:

The present invention provides a method and system for providing a semiconductor device. The semiconductor device includes a first layer to be etched. The method and system comprise depositing an anti-reflective coating ~~(ARC)~~. The method and system also comprise patterning a resist layer, the resist layer has a pattern including a plurality of apertures therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ~~ARC~~ anti-reflective coating layer are exposed by the pattern. The method and system also comprise etching the first portion of the first layer and the second portion of the ~~ARC~~ anti-reflective coating layer and removing the resist layer utilizing a plasma etch. The ~~ARC~~ anti-reflective coating layer is resistant to the plasma etch.

Please replace the paragraph beginning at line 6, page 6 with the following rewritten paragraph:

According to the system and method disclosed herein, the present invention reduces the removal of the ~~ARC~~ anti-reflective coating layer by using a plasma etch to strip photoresist. The ~~ARC~~ anti-reflective coating layer is resistant to removal by the plasma etch. Consequently, the ~~ARC~~ anti-reflective coating properties of the ~~ARC~~ anti-reflective coating layer are preserved, allowing a reduction in the swing curve effect and reflective notching.

Please replace the paragraph beginning at line 22, page 6 and ending at line 1, page 7 with the following rewritten paragraph:

Figure 4A is a flow chart depicting one embodiment of a method for providing a portion of a semiconductor device and an ~~ARC~~ anti-reflective coating layer in accordance with the present invention.

Please replace the paragraph beginning at line 20, page 7 and ending at line 6, page 8 with the following rewritten paragraph:

Conventional semiconductor devices are typically processed using conventional anti-reflective coating ~~(ARC)~~ layers. For example, a conventional semiconductor device, such as an embedded flash memory, contains a logic region and a memory region. In order to pattern gates with a narrow distribution of the critical dimension in the logic region and the memory region, a conventional ~~ARC~~ anti-reflective coating layer is deposited on a polysilicon layer. The conventional ~~ARC~~ anti-reflective coating layer is typically SiON. The anti-reflective properties of the conventional ~~ARC~~ anti-reflective coating layer are highly dependent on the thickness of the conventional ~~ARC~~ anti-reflective coating layer. Typically, the conventional ~~ARC~~ anti-reflective coating layer has a desired thickness of three hundred Angstroms plus or minus approximately thirty Angstroms thick. Outside of

the desired thickness, the conventional ~~ARC~~ anti-reflective coating layer may not adequately reduce or prevent reflections.

Please replace the paragraph beginning at line 7, page 8 with the following rewritten paragraph:

Typically, the conventional ~~ARC~~ anti-reflective coating layer is deposited with the desired thickness. The gates in the memory portion of the conventional ~~imbedded~~ embedded memory are then patterned. Typically, this includes patterning a first layer of photoresist and etching the polysilicon and conventional ~~ARC~~ anti-reflective coating layer. The first layer of photoresist completely covers the logic region of the conventional memory and is patterned in the memory region. After the stacked gates are etched, the first photoresist layer is stripped using a wet chemical. The gates in the logic portion of the conventional ~~imbedded~~ embedded memory are then patterned. This step is typically performed by patterning a second photoresist layer and etching the polysilicon and conventional ~~ARC~~ anti-reflective coating layer under apertures in the second photoresist layer. For this step, the second photoresist layer typically covers the memory region and is patterned in the logic region of the conventional ~~imbedded~~ embedded memory. Thus, the gates in the memory region and the gates in the logic region are processed independently.

Please replace the paragraph beginning at line 19, page 8 and ending at line 4, page 9 with the following rewritten paragraph:

The stripping of the photoresist structure after gates in the memory region are formed using the first etch removes a significant portion of the conventional ~~ARC~~ anti-reflective coating layer, typically twenty to fifty Angstroms. The desired thickness of the conventional ~~ARC~~ anti-reflective coating layer is approximately three hundred Angstroms plus or minus about ten percent. Thus, removal of a portion of the conventional ~~ARC~~ anti-reflective coating layer during the photoresist strip may

take the conventional ~~ARC~~ anti-reflective coating layer far enough away from the desired thickness that the conventional ~~ARC~~ anti-reflective coating layer is no longer efficient. Thus, when the structures, such as gates, in the logic region are formed, the critical dimension of the structures varies greatly due to the swing curve effect and reflective notching.

Please replace the paragraph beginning at line 5, page 9 with the following rewritten paragraph:

One method for remedying this would be to deposit a thicker conventional ~~ARC~~ anti-reflective coating layer at the outset. Once the first photoresist structure is stripped, the conventional ~~ARC~~ anti-reflective coating layer would have the desired thickness. Variations of the critical dimensions of structures in the logic region due to the swing curve effect would be reduced. However, because the conventional ~~ARC~~ anti-reflective coating layer was thicker as provided, the conventional ~~ARC~~ anti-reflective coating layer might not function properly for processing of the memory region. Thus, variations in the critical dimensions of structures in the memory region due to the swing curve effect or reflective notching would be greatly increased.

Please replace the paragraph beginning at line 13, page 9 with the following rewritten paragraph:

The present invention provides a method and system for providing a semiconductor device. The semiconductor device includes a first layer to be etched. The method and system comprise depositing an anti-reflective coating ~~(ARC)~~. The method and system also comprise patterning a resist layer. The resist layer has a pattern including a plurality of apertures therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ~~ARC~~ anti-reflective coating layer are exposed by the pattern. The method and system also comprise etching the first portion of the first layer and the second portion of the ~~ARC~~

anti-reflective coating layer and removing the resist layer utilizing a plasma etch. The ~~ARC~~ anti-reflective coating layer is resistant to the plasma etch.

Please replace the paragraph beginning at line 7, page 10 and ending at line 11, page 11 with the following rewritten paragraph:

To more particularly illustrate the method and system in accordance with the present invention, refer now to Figure 4A, depicting one embodiment of a method 100 in accordance with the present invention for providing a semiconductor device such as an embedded memory. The memory 100 preferably commences after a first layer to be etched has been provided. In a preferred embodiment, the method 100 commences after a polysilicon layer desired to be patterned has been deposited. The polysilicon layer is to be patterned into stacked gates and logic gates. An ~~ARC~~ anti-reflective coating layer of a desired thickness is provided, preferably by depositing the ~~ARC~~ anti-reflective coating layer, via step 102. Preferably, the ~~ARC~~ anti-reflective coating layer deposited in step 102 is a SiON layer. Also in a preferred embodiment, the desired thickness of the ~~ARC~~ anti-reflective coating layer is the thickness desired for maximizing the anti-reflective properties of the ~~ARC~~ anti-reflective coating layer. In one embodiment, this thickness is three hundred Angstroms plus or minus ten percent. However, the ~~ARC~~ anti-reflective coating layer may have another desired thickness. For example, in some other applications, the desired thickness of the ~~ARC~~ anti-reflective coating layer may be one hundred to five hundred Angstroms. A photoresist layer is then patterned on the ~~ARC~~ anti-reflective coating layer, via step 104. The photoresist structure includes a pattern which has apertures over the regions desired to be etched and covers regions desired to be preserved. The ~~ARC~~ anti-reflective coating layer and underlying first layer are then etched, via step 104. Because the ~~ARC~~ anti-reflective coating layer has the desired thickness, variations in the critical dimensions of structures etched into the first layer due to variations in the thickness of the photoresist structure are reduced. Thus, gates may be formed in a region of the embedded memory. The photoresist layer is then

etched using a plasma etch to which the ~~ARC~~ anti-reflective coating layer is resistant, via step 108. Thus, the ~~ARC~~ anti-reflective coating layer is resistant to removal by the plasma etch. In contrast, the photoresist structure is layer by the plasma etch. In other words, the selectivity of the etch for the photoresist is relatively high, while the selectivity of the etch for the ~~ARC~~ anti-reflective coating layer is relatively low. Consequently, little or none of the ~~ARC~~ anti-reflective coating layer is removed when the photoresist structure is removed. Because the ~~ARC~~ anti-reflective coating layer is protected from removal, the anti-reflective properties of the ~~ARC~~ anti-reflective coating layer are preserved for later use. As a result, the critical dimensions of the structures formed using the ~~ARC~~ anti-reflective coating layer after removal of the photoresist structure will not vary greatly due to the swing curve effect.

Please replace the paragraph beginning at line 12, page 11 and ending at line 8, page 12 with the following rewritten paragraph:

Figure 4B depicts a more detailed flow chart of a method for providing a portion of a semiconductor device, such as an embedded memory, which has a logic region and a memory region. A polysilicon layer is deposited on a semiconductor substrate, via step 112. The polysilicon layer is analogous to the first layer discussed with respect to Figure 4A. The polysilicon layer is to be patterned into the stacked and logic gates. Referring back to Figure 4B, a SiON ~~ARC~~ anti-reflective coating layer is deposited at the desired thickness for anti-reflective properties of the SiON ~~ARC~~ anti-reflective coating layer, via step 114. In a preferred embodiment, the desired thickness is approximately three hundred Angstroms plus or minus approximately thirty Angstroms. A first resist structure is then patterned, via step 116. Preferably, step 116 includes spin-coating photoresist on the embedded memory and developing a pattern in the photoresist using photolithography. The first resist layer includes a pattern that has apertures over a first region and covers a second region. Thus, the first resist structure is for fabricating structures in the first region of the embedded memory. In a preferred embodiment, the first resist structure is for

providing stacked gates in the memory region of the embedded memory. Thus, in a preferred embodiment, the first region of the embedded memory is the memory region. The structures in the first region are then defined using an etch, via step 118. The first photoresist structure is then stripped using a plasma etch that uses a plasma including a forming gas, via step 120. The plasma used in step 120 thus etches the photoresist. However, the ~~ARC~~ anti-reflective coating layer is resistant to removal by the plasma used in step 120. Consequently, the photoresist strip performed in step 120 removes little or none of the ~~ARC~~ anti-reflective coating layer.

Please replace the paragraph beginning at line 9, page 12 with the following rewritten paragraph:

An optional wet preclean, for example using sulfuric acid, may then be performed, via step 122. The wet preclean removes any remaining residues from the plasma etch performed in step 122. Although the ~~ARC~~ anti-reflective coating layer is exposed to the wet etchant in the wet preclean, the preclean is only used to remove residues. Consequently, exposure of the ~~ARC~~ anti-reflective coating layer to the wet etchant is greatly reduced. Thus, the amount of the ~~ARC~~ anti-reflective coating layer removed by the wet etchant is still greatly reduced over the amount of the ~~ARC~~ anti-reflective coating layer removed by a conventional photoresist strip.

Please replace the paragraph beginning at line 16, page 12 and ending at line 5, page 13 with the following rewritten paragraph:

A second resist layer for a second portion of the semiconductor device is then patterned, via step 124. Preferably, step 124 includes spin-coating photoresist ont eh embedded memory and developing a pattern in the photoresist using photolithography. The second resist layer has a pattern including apertures over the second region and covers the first region. Thus, the second resist layer is for fabricating structures in the second region of the embedded memory. In a preferred

embodiment, the second resist layer is for providing gates in the logic region of the embedded memory. Thus, in a preferred embodiment, the second region of the embedded memory is the logic region. The structures in the second region of the semiconductor device are then etched, via step 126. Thus, gates in the logic region may be defined in step 126. Processing of the embedded memory may be completed, via step 128. Step 128 thus includes stripping the second photoresist layer and performing any subsequent processing steps. Step 128 may also include removing the ~~ARC~~ anti-reflective coating layer prior to formation of subsequent structures.

Please replace the paragraph beginning at line 6, page 13 with the following rewritten paragraph:

Because the photoresist is stripped using a plasma etch to which the ~~ARC~~ anti-reflective coating layer is resistant, the ~~ARC~~ anti-reflective coating layer is less susceptible to removal by the photoresist strip in accordance with the present invention. In one embodiment, the photoresist strip in accordance with the present invention does not remove any of the ~~ARC~~ anti-reflective coating layer. In another embodiment, a photoresist strip removes in accordance with the present invention only a small portion of the ~~ARC~~ anti-reflective coating layer. This portion is small enough to allow the ~~ARC~~ anti-reflective coating layer to continue to act as an anti-relfective layer. The preservation of most or all fo the ~~ARC~~ anti-reflective coating layer is in contrast to removal of ten to twenty Angstroms of a conventional ~~ARC~~ anti-reflective coating layer using a conventional wet photoresist strip. Because the ~~ARC~~ anti-reflective coating layer is less subject to removal by a photoresist strip in accordance with the present invention, the thickness of the ~~ARC~~ anti-reflective coating layer is preserved for fabrication of structures in the second portions of a semiconductor device. The ~~ARC~~ anti-reflective coating layer can thus still reduce the variation of the critical dimensions of structures fabricated. Furthermore, because the ~~ARC~~ anti-reflective coating layer has the desired thickness as provided, the variations in the critical dimensions of structures fabricated in the first region are also reduced.

For example, the stacked gates of the memory region and the gates of the logic region can both be formed without being subject to wide variations in critical dimension due to the swing curve effect. Consequently, processing of a semiconductor device, such as an embedded memory, is facilitated.

Please replace the paragraph beginning at line 1, page 14 with the following rewritten paragraph:

For example, refer to Figures 5A-5C, depicting an embedded memory 200 during processing in accordance with the methods 100 or 110. Figure 5A depicts the embedded memory 200 after step 104 or 116 of patterning the first photoresist structure has been performed. The embedded memory 200 includes a memory region 202 and a logic region 204. A polysilicon layer 212 has been deposited on a substrate 210. The polysilicon layer 212 is generally separated from the substrate 210 by a thin insulating layer (not shown). In addition, underlying structure 201 and 203 in the logic and memory regions, respectively, are shown. The ~~ARC~~ anti-reflective coating layer 214 has been provided on the polysilicon layer 212 at the desired thickness. The photoresist structure 216 has also been provided. The photoresist structure 216 includes apertures exposing the ~~ARC~~ anti-reflective coating layer 214 and the underlying polysilicon layer 212.

Please replace the paragraph beginning at line 11, page 14 with the following rewritten paragraph:

Figure 5B depicts the semiconductor device 200 after the first resist layer has been stripped using a photoresist strip in accordance with the present invention, such as in steps 108 or 120. The stacked gates 220, 222 and 224 have been provided in the memory region 202. Because of the etching, only portions 221, 223 and 225 of the ~~ARC~~ anti-reflective coating layer 214 remain in the memory region 202. Because the ~~ARC~~ anti-reflective coating layer was deposited at approximately the desired

thickness, the stacked gates 220, 222 and 224 have critical dimensions close to what is desired. Thus, the ~~ARC~~ anti-reflective coating layer 214 has greatly reduced the swing curve effect in the memory region. No structures have been formed in the logic region 202. Furthermore, the resist strip using the plasma etch has not greatly affected the thickness of the ~~ARC~~ anti-reflective coating layer 214 because the ~~ARC~~ anti-reflective coating layer is resistant to removal by the plasma etch. Consequently, the ~~ARC~~ anti-reflective coating layer 214 still retains sufficient anti-reflective properties to be used in fabricating structures in the logic region 204.

Please replace the paragraph beginning at line 1, page 14 and ending at line 5, page 15 with the following rewritten paragraph:

Figure 5C depicts the semiconductor device 200 after removal of the second resist structure. Thus, the gates 230, 232 and 234 have been defined in the logic region 204. Because of the presence of the ~~ARC~~ anti-reflective coating layer 214, remaining as regions 231, 233 and 235, the critical dimensions of structures in the logic region 204 do not vary greatly. Thus, the swing curve effect has been greatly reduced in the logic region 204 of the embedded memory 200. Thus, processing of the embedded memory 200 is facilitated.

Please replace the paragraph beginning at line 6, page 15 with the following rewritten paragraph:

A method and system has been disclosed for using a plasma etch, which an ~~ARC~~ anti-reflective coating layer is resistant to, in order to remove a photoresist structure. Thus, the ~~ARC~~ anti-reflective coating layer is preserved for subsequent use. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be

made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

Please replace the Abstract beginning at line 2, page 19 and ending at line 10, page 19 with the following rewritten paragraph:

A method and system for providing a semiconductor device ~~is disclosed~~. The semiconductor device includes a first layer to be etched. The method and system include depositing an anti-reflective coating ~~(ARC)~~. At least a portion of the ~~ARC~~ anti-reflective coating layer is on the first layer. The method and system also include patterning a resist layer. The resist layer includes a pattern having a plurality of apertures therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ~~ARC~~ anti-reflective coating layer are exposed by the pattern. The method and system also include etching the first portion of the first layer and the second portion of the ~~ARC~~ anti-reflective coating layer and removing the resist layer utilizing a plasma etch. The ~~ARC~~ anti-reflective coating layer is resistant to the plasma etch.